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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
CHANG, ERIC

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/504,003	KAHN ET AL.	
	Examiner	Art Unit	
	Eric Chang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-25 are pending.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "A METHOD AND APPARATUS FOR RESUMING MEMORY OPERATIONS FROM A LOW LATENCY WAKE-UP LOW POWER STATE".

4. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

5. The use of the trademark Rambus has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-5, 7-9, 18-21 and 24 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by U.S. Patent 6,230,274 to Stephens et al.

8. As to claim 1, Stephens discloses an apparatus comprising:

[a] a processor [col. 21, line 40];

[b] an operating system to control a plurality of power management states, comprising a low latency low power state [col. 1, lines 26-32];

[c] a memory subsystem that requires initialization commands to exit a memory low power state [col. 1, lines 66 and col. 2, lines 1-2]; and

[d] control logic to detect exiting of said low latency low power state [col. 21, line 11] and to execute initialization commands to remove said memory subsystem from said memory low power state prior to allowing execution of processor to resume [col. 21, lines 16-20].

9. As to claims 2 and 3, Stephens discloses the low latency low power state is an ACPI S1 state [col. 1, lines 26-44] and said memory low power state is one of a nap and powerdown state [col. 19, lines 4-7]. Stephens teaches the low power state may be any one of the ACPI sleep states and that the memory is capable of nap and powerdown state, substantially as claimed. Furthermore, it is obvious to one of ordinary skill in the art that exiting from the ACPI S1 state occurs comprises resumption of execution without executing BIOS routines.

10. As to claim 4, Stephens discloses control logic comprising of:

[a] low power state exit detection logic [col. 21, line 11]; and

[b] memory resume sequencing logic [col. 21, lines 16-20].

Because Stephens teaches a control logic that both detects a lower power state exit and resumes memory operation, Stephens teaches the component logics that perform the tasks individually.

11. As to claims 5 and 24, Stephens discloses the memory resuming logic allows the deassertion of a stop clock signal after said plurality of initialization commands have been

executed [col. 21, lines 21-23]. Stephens teaches re-starting the clock, which comprises deasserting the stop clock signal that was asserted when the processor entered the ACPI sleep mode.

12. As to claims 7 and 19, Stephens discloses the initialization commands comprise:

[a] initializing memory interface control logic [col. 21, line 24];

[b] starting a clock [col. 21, lines 23];

[c] performing a current calibration sequence [col. 21, lines 27-28]; and

[d] performing memory core initialization operations [col. 21, lines 25-26].

Furthermore, Stephens teaches starting the clock comprises waiting for the clock circuit to lock [col. 12, lines 5-6], and that performing a current calibration sequence comprises setting a control current register [col. 16, lines 28-31], substantially as claimed.

13. As to claims 8 and 20, Stephens discloses setting the current control register to a midpoint value [col. 16, lines 33-40].

14. As to claims 9 and 21, Stephens discloses the core initialization comprises performing a series of pre-charge and refresh operations [col. 16, lines 41-50].

15. As to claim 18, Stephens discloses a method comprising:

[a] detecting an event to cause an exit from a low latency low power state [col. 21, line 11];

[b] exiting the low power low latency state [col. 21, lines 12-37].

Furthermore, Stephens teaches that the initialization of the memory subsystem is performed automatically by the memory interface, and is therefore performed transparently to an operating system, substantially as claimed.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 6, 10-17, 22-23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,230,274 to Stephens et al. in view of U.S. Patent 6,272,642 to Pole, II et al.

18. As to claim 6, Stephens teaches all of the limitations of the claim, including the low power state exit detection logic [col. 21, line 11] and the memory resume logic [col. 21, lines 16-20] in the ICH and the memory interface, respectively. Stephens also teaches a low power state exit message [col. 8, line 67 and col. 9, line 1] and signaling that the memory interface has completed its initialization commands [col. 4, lines 30-33], but does not specifically teach the messaging logic between the ICH and the memory interface.

Pole teaches that messages, such as those pertaining to placing the system into sleep modes, may be used to communicate between memory and I/O hubs [col. 4, lines 10-21]. Thus,

Pole teaches logic for transmitting messages indicating the claimed contents, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the messaging system as taught by Pole. One of ordinary skill in the art would have been motivated to do so that the memory interface and the ICH are able to communicate with each other.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of communicating sleep commands between a memory interface and an ICH. Moreover, the messaging means taught by Pole would improve the flexibility of Stephens because it allowed direct messaging between the memory interface and the ICH instead of relying on polling a completion register or on direct signals between the two components.

19. As to claims 10-13, Stephens discloses:

[a] low power state exit detection logic [col. 21, line 11];

[b] memory resume logic [col. 21, lines 16-20];

[c] signaling that the memory interface has completed its initialization commands [col. 4, lines 30-33];

[d] low power state exit message [col. 8, line 67 and col. 9, line 1]; and

[e] memory resuming logic that deasserts a stop clock signal after said plurality of initialization commands have been executed [col. 21, lines 21-23].

Stephens teaches all of the limitations of the claim, but does not specifically teach the messaging logic between the ICH and the memory interface.

Pole teaches that messages, such as those pertaining to placing the system into sleep modes, may be used to communicate between memory and I/O hubs [col. 4, lines 10-21]. Thus, Pole teaches logic for transmitting messages indicating the claimed contents, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the messaging system as taught by Pole. One of ordinary skill in the art would have been motivated to do so that the memory interface and the ICH are able to communicate with each other.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of communicating sleep commands between a memory interface and an ICH. Moreover, the messaging means taught by Pole would improve the flexibility of Stephens because it allowed direct messaging between the memory interface and the ICH instead of relying on polling a completion register or on direct signals between the two components.

20. As to claim 14, Stephens discloses the low latency low power state may be any one of the ACPI sleep states, such states comprising the S1 state [col. 1, lines 26-44].

21. As to claim 15, Stephens discloses the initialization commands comprise:

[a] initializing memory interface control logic [col. 21, line 24];

[b] starting a clock [col. 21, lines 23];

[c] performing a current calibration sequence [col. 21, lines 27-28]; and

[d] performing memory core initialization operations [col. 21, lines 25-26].

Furthermore, Stephens teaches starting the clock comprises waiting for the clock circuit to lock [col. 12, lines 5-6], and that performing a current calibration sequence comprises setting a control current register [col. 16, lines 28-31], substantially as claimed.

22. As to claim 16, Stephens discloses setting the current control register to a midpoint value [col. 16, lines 33-40].

23. As to claim 17, Stephens discloses the core initialization comprises performing a series of pre-charge and refresh operations [col. 16, lines 41-50].

24. As to claim 22, Pole discloses

[a] reading a bit set by BIOS upon entry into a low latency low power state [col. 7, lines 51-55]; and

[b] sending a resume message from an ICH to memory interface logic [col. 8, lines 25-32].

Pole teaches that messages may be used to communicate between memory and I/O hubs in lieu of signals [col. 4, lines 10-21]. Thus, Pole teaches logic for transmitting messages indicating the detection of an exit from the low power state, substantially as claimed.

25. As to claim 23, Stephens discloses:

[a] signaling that the memory interface has completed its initialization commands [col. 4, lines 30-33];

[b] deasserting a stop clock signal [col. 21, lines 21-23].

26. As to claim 25, Pole discloses:

[a] detecting a low power state entry [col. 1, lines 36-38]; and

[b] setting a bit to indicate the low latency low power state is selected [col. 6, lines 61-67].

Pole teaches writing a pre-defined value to a control register to indicate the new power state of the processor; this can comprise setting a bit to indicate said selected power state.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
September 24, 2002

THOMAS LEE
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